**Amendments to the Claims**

Claims 1-25 (Canceled).

26. (Previously Presented): Memory circuitry comprising:

a semiconductor substrate;

a plurality of word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer comprising at least a single well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within said single well over the word lines;

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array; and

the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

27. (Original): The memory circuitry of claim 26 wherein the base is substantially planar.

28. (Original): The memory circuitry of claim 26 wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

29. (Original): The memory circuitry of claim 26 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

30. (Original): The memory circuitry of claim 26 comprising buried digit lines and wherein the base is substantially planar, and the well base being received at least 1000 Angstroms above outermost tops of the digit lines.

Claim 31. (Canceled).

32. (Previously Presented): The memory circuitry of claim 26 wherein the capacitor storage node electrodes have topmost surfaces which are received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

33. (Previously Presented): Memory circuitry comprising:

a semiconductor substrate;

an insulative layer received over the substrate, the insulative layer comprising at least a single well formed therein, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a base, an oxygen diffusion barrier layer received over the well base;

a plurality of memory cell storage capacitors received within said single well, the memory cell storage capacitors respectively comprising a storage node container which is received within the insulative layer through the oxygen diffusion barrier layer and through the well base; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

34. (Previously Presented): The memory circuitry of claim 33 comprising word lines, wherein the word lines have insulative caps and the well base has a lowest portion which is received at least 2000 Angstroms above the caps.

35. (Original): The memory circuitry of claim 33 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

36. (Original): The memory circuitry of claim 33 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

37. (Original): The memory circuitry of claim 33 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

Claims 38-47 (Canceled).

48. (Currently Amended): The memory circuitry of ~~claim 26~~ claim 33 wherein the oxygen diffusion barrier layer received over the well base comprises ~~Si3N4~~ $Si_3N_4$.

49. (Currently Amended): The memory circuitry of claim 48 wherein the ~~Si3N4~~ $Si_3N_4$ comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

50. (Currently Amended): The memory circuitry of claim 48 wherein the ~~Si3N4~~ $Si_3N_4$ comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.

51. (Currently Amended): The memory circuitry of ~~claim 33~~ claim 26 wherein the insulative layer comprises ~~SiO2~~ $SiO_2$, and further comprising an ~~Si3N4~~ $Si_3N_4$ comprising layer received on the well base.

52. (Currently Amended): The memory circuitry of claim 51 wherein the ~~Si3N4~~ $Si_3N_4$ comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

53. (Currently Amended): The memory circuitry of claim 51 wherein the ~~Si3N4~~ $Si_3N_4$ comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.

54. (Previously Presented): The memory circuitry of claim 26 wherein individual of the capacitors have a storage node electrode, one of the storage node electrodes being spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.

55. (Previously Presented): The memory circuitry of claim 33 wherein the respective storage node containers are spaced laterally inward of the outline peripherally defined by the well thereby forming respective spaces between said containers and said outline.

56. (Previously Presented): The memory circuitry of claim 33 wherein the base is substantially planar.

57. (Previously Presented): The memory circuitry of claim 33 wherein the insulative layer is formed to have a substantially planar outermost surface, the memory cell storage capacitors respectively comprising an outer cell electrode having a topmost surface which is received elevationally outward of the insulative layer.

58. (Previously Presented): The memory circuitry of claim 26 wherein the memory cell storage capacitors respectively comprise an outer cell electrode having a topmost surface which is received elevationally outward of the insulative layer.

59. (New): The memory circuitry of claim 48 wherein the $Si_3N_4$ comprising oxygen diffusion barrier layer is received on the well base.